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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,665	05/21/2004	Hsin-Wo Fang	NAUP0592USA	3664

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
06/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,665	FANG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-10, 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/709,665 filed 05/21/2004 and amendment filed 04/03/2007.

2. Claims 1-3, 5-10, 12-15 remain pending in the Application. Claims 4 and 11 have been cancelled from the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/03/2007 as been entered.

Claim Objections

4. Claims 1 and 9 are objected to because of the following informalities: the wherein clause of the second limitation of the claims 1 and 9 is formulated unclear, such as "each **layout** in the connection layer corresponding to each sub-circuit cell **is** selectively **connected to the sub-circuit blocks of each sub-circuit cell** ...", i.e. it is not clear what is connected to what. For the examination purposed Examiner's interpretation is: connections between sub-circuits.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5, 7-10, 12, 14, 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Schadt et al. (US Patent 6,870,395).

With respect to claim 1 Schadt et al. teaches a method for implementing circuit layouts in a chip (within a layout of the chip/PLD shown on the Fig. 2 (col. 3, ll.31-32)), comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip, where each sub-circuit cell comprising at least two types of sub-circuit blocks (within plurality of standard-cell logic blocks (SLBs) 220 as shown on the Fig. 2 (col. 3, ll.40-42), wherein SLBs are construed by same type of standard-cell logic, i.e. having the same layout (col. 4, ll.3-5) and are placed in different positions of the PLD (col. 4, ll.9-10), wherein each SLB contains plurality of small blocks (col. 4, ll.2-4; ll.42-43) and wherein SLBs contain plurality of gates which might be two types, such as I/O receive gates and I/O transmit gates (col. 11, ll.17-20; col. 5, ll.45-49)); and

when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells, wherein each layout in the connection layer corresponding to each sub-circuit cell so that the sub-circuit cells in different

positions implement different circuit functions (within placing SLBs in different areas of PLD depending on the functionality to be supported (col. 4, ll.6-8) and using two types of connectivity structure in order to integrated SLBs with the rest of the chip (col. 4, ll.42-44), wherein both types of connectivity structure are using upper layer of metallization (metal layer) programmably connect each SLB to the other portions of the chip/PLD as shown on the Fig. 9 (col. 4, ll.44-56), wherein SLBs having routing resources provide programmable connections between each SLBs and any of the I/O circuitry and other components of the circuit (col. 2, ll.4-6) and wherein SLB routing resources, within different number of wires connecting standard gates, give the opportunity to perform different function (without changing the layout of the SLB) of SLB (col. 5, ll.23-26; col. 9, ll.26-28; ll.43-47)).

With respect to claim 9 Schadt et al. teaches a chip (within a layout of the chip/PLD shown on the Fig. 2 (col. 3, ll.31-32)), comprising:

a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout, each sub-circuit cell comprising at least two types of sub-circuit blocks (within multilayered PLD (col. 4, ll.53-54) containing plurality of SLBs 220 as shown on the Fig. 2 having the same layout of standard-cell blocks in different positions of the PLD 200 around the periphery of the device (i.e. within I/O ring) (col. 3, ll.40-42), wherein SLBs can placed anywhere within PLD/chip (col. 4, ll.9-10) and wherein SLBs contain plurality of gates which

might be two types, such as I/O receive gates and I/O transmit gates (col. 11, ll.17-20; col. 5, ll.45-49)); and

at least a connection layer comprising different layouts corresponding to the different positions of the layout layers, wherein each layout of the connection layer selectively connects the sub-circuit blocks of each corresponding sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions (within programmable connection of each SLB with the other portions of the PLD (col. 4, ll.51-53) using metal layers of the PLD (col. 4, ll.53-55) depending on the available area and the functionality to be supported (col. 4, ll.6-8), wherein SLBs having routing resources provide programmable connections between SLBs and any of the I/O circuitry and other components of the circuit (col. 2, ll.4-6) and wherein SLB routing resources, within different number of wires connecting standard gates, give the opportunity to perform different function (without changing the layout of the SLB) of SLB (col. 5, ll.23-26; col. 9, ll.26-28; ll.43-47)).

With respect to claims 2-5, 7, 8, 10-12, 14 and 15 Schadt et al. teaches:

Claims 2, 10: wherein the connection layer is a metal layer (col. 4, ll.53-55);

Claim 3: the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer (within SLBs construed by the same type of standard-cell logic blocks (col. 4, ll.4-6), wherein in order to support different

functions SLBs have programmable connectivity structure (col. 4, ll.44-52) without changing the layout of SLBs));

Claims 5, 12: wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions (using plurality of SLBs positioned around the periphery of the device layout, i.e. in the I/O ring (col. 1, ll.51-53) for performing programmable connections between I/O circuitry and the programmable core logic of the chip (col. 2, ll.1-3);

Claims 7, 14: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates (within different type of SLBs performing different functions (col. 9, ll.26-27; ll.43-47; col. 10, ll.58-67));

Claims 8, 15: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents (within different type of SLBs performing different functions (col. 9, ll.26-27; ll.43-47; col. 10, ll.58-67)).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schadt et al. as applied to claims 1 and 9 above, and further in view of Maeda (US Patent 6,052,014).

With respect to claims 6 and 13 Schadt et al. teaches the limitation from which claims depend including SLBs being placed at any position in the layout of the integrate circuit in the input/output ring area implementing multiple functions based on the routing resources of the SLB (I/O circuit) (not changing the layout of the SLB). However Schadt et al. lacks specifics regarding implementing a Schmidt trigger function by I/O circuit. Maeda teaches:

Claims 6, 13: wherein the sub-circuit cells in different positions are for implementing I/O circuit with a Schmidt trigger function (col. 1, ll.59-63). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Maeda to teach the specifics subject matter Schadt et al. does not teach, because there is an ability of transferring signals of different voltage levels between the internal circuit and the circuits constructing the input/output circuit and performing slew rate control (abstract of Maeda).

Remarks

9. In remarks Applicant argues in substance:

a) First, the method of the present application programmably connects different types of sub-circuit blocks in the same sub-circuit to achieve different circuit functions, while Schadt's method requires to connect the SLB's to other portion of the PLD e.g. I/O buffers or memory blocks.

b) Second, the programming of the present application is achieved only by changing the layout of the connection layer. On the other hand, Schadt,s method requires using muxes and software control to implement different functions.

10. Examiner respectfully disagrees for the following reasons:

With respect to a) Schadt et al. teaches SLBs having routing resources provide programmable connections between SLBs and any of the I/O circuitry and other components of the circuit (col. 2, ll.4-6) and wherein SLB routing resources, within different number of wires connecting standard gates, give the opportunity to perform different function of SLB (col. 5, ll.23-26; col. 9, ll.26-28; ll.43-47), wherein the routing resources of SLBs are implemented on the metal/interconnection layers to define the function of SLB to be performed (col. 4, ll.53-55).

With respect to b) Schadt et al. teaches SLB routing resources provide programmable connections between SLB,s and between SLBs and any of the I/O circuitry or other components (col. 2, ll.4-6), wherein programmable the routing resources of SLBs are implemented on the metal/interconnection layers to define desired function of SLB to be performed (col. 4, ll.53-55; col. 5, ll.24-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
06/15/2007

Helen Rossoshek
Examiner
Art Unit 2825